

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)	
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Shibly S. Ahmed et al.)	Group Art Unit: Unassigned
)	
Application No.: Unassigned)	Examiner: Unassigned
)	
Filed: December 4, 2003)	
)	
Title: DAMASCENE GATE SEMICONDUCTOR)	
PROCESSING WITH LOCAL THINNING)	
OF CHANNEL REGION)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicant(s) bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement is being filed before the mailing date of a first Office Action in the above-referenced application. As such, no certification or fee is required. Copies of the listed documents, except for U.S. patents and U.S. patent publications, are attached.

Applicant(s) respectfully request(s) that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

If any copending application(s) is/are cited on the attached PTO 1449, the Examiner's attention is directed to the foregoing application(s) in compliance with § 2001.06(b) of the Manual of Patent Examining Procedure. By identifying the copending application(s), the assignee and/or applicant of the application(s) do not waive confidentiality of the application(s). Accordingly, the U.S. Patent and Trademark Office is requested to maintain the confidentiality of the copending application(s) under 35 U.S.C. § 122.

This submission does not represent that a search has been made and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicant(s) determine(s) that the cited document(s) do not constitute "prior art" under United States law, Applicant(s) reserve(s) the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

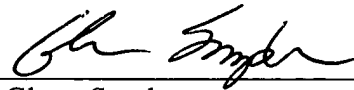
Applicant(s) further reserve(s) the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 50-1070.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By:



Glenn Snyder
Reg. No. 41,428

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800
Customer Number: 26615

Date: December 4, 2003

INFORMATION DISCLOSURE CITATION PTO-1449	Customer Number 26615	ATTORNEY'S DKT NO. H1478		APPLICATION NO. Unassigned	
		APPLICANT(S) Shibly S. Ahmed et al.			
		FILING DATE DECEMBER 4, 2003		GROUP Unassigned	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,225,173 B1	05-01-01	Yu	438	301	11-06-98
	6,413,802 B1	07-02-02	Hu et al.	438	151	10-23-00
	6,583,469 B1	06-24-03	Fried et al.	257	329	01-28-02

FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Co-pending U.S. Patent Application No. 10/405,342, filed April 3, 2003 entitled: "Method for Forming a Gate in a FinFet Device and Thinning a Fin in a Channel Region of the FinFet Device," 17 page specification; 14 sheets of drawings.
	Digh Hisamoto et al.: "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
	Yang-Kyu Choi et al.: "Sub-20nm CMOS Fin FET Technologies," 2001 IEEE, IEDM, pages 421-424.
	Xuejue Huang et al.: "Sub-50 nm P-Channel Fin FET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
	Yang-Kyu Choi et al.: "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
	Xuejue Huang et al.: "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).